ELT-217, **Experiment AD9**: Shift Register Operation

EQUIPMENT NEEDED:

Analog Discovery unit and computer
74LS194 IC
Breadboard and wires

GENERAL & BACKGROUND:

The '194 is a 4-bit bi-directional parallel-in, parallel-out, shift register with a master clear. The function is determined by the two mode control inputs S_0 and S_1. Data shifts or is loaded in on the leading (rising) edge of the clock pulse. See the manufacturer's data sheet.

B**efore** actually wiring, make a schematic diagram showing which AD2 switch number is connected to what; show all connections and pin numbers. Include diagrams in your report for each different set-up. Where data is in ordered words your switches and LEDs should be chosen so that they appear on the control panel in shifted bit order, *for example*: $D_a..D_b..D_c..D_d$

PROCEDURE:

(1) Make a wiring diagram, with all pin numbers indicated, **and** a connection table, to meet the specifications below. Once you have completed the wiring diagram and table, and have had it approved, you will be given the 74LS194 IC. The wiring diagram and connection table must be included in your report. A suggested format of the connection table is given in figure 1, below.

The following connections should be shown on the diagram: The clock pulse is fed by an AD2 push button set to go from low to high when pushed. The clear input is fed by an AD2 push buttons set to go from high to low when pushed. The two mode (S1 and S0) control lines and the two serial-data-in (left and right) go to 4 data switches which can be set either high or low. The four parallel-in lines (A, B, C, D) go, in order A-D, to 4 data switches which can be set either high or low. The parallel outputs (Q_A - Q_D) go to four LEDs, in order A-D.

Figure 1. Suggested connection table.

IC Functions	INPUTS										OUTPUTS			
	clear	clock	mode		Serial		Parallel				QA	QB	QC	QD
			S1	S0	left	right	A	B	C	D				
AD2 I/O #														
AD2 lead color														
IC pin #														

Wiring diagram approved _____ (Instr. initial and date)

(2) Construct the circuit based on your wiring diagram.

(Remember when taking data to take screen shots for the results of each step.)

(3) Parallel Entry of Data for the '194

(a) Start out with mode control lines set for parallel data entry (both high).

(b) Set the input data input switches to produce 1101 (or other appropriate data) on the inputs. Observe if the outputs change as the switches are set. Would you expect any change?

(c) You then must clock the data into the register flip-flops. Do this by momentarily pushing the clock button so it goes high and then low again. Confirm that the outputs are what is expected.

Whenever it is necessary to load data into the '194 shift register in parallel, refer to this procedure outlined above.

(4) Shift Right Serial Output for the '194

(a) With the data 1101 loaded into the register as in (3), above, set the mode to shift right (S_1=low, S_0=high), and set the right serial input to LOW. Pulse the clock input six times. Record and screen shot the Q_A - Q_D outputs at the start and after each pulse.

(b) Re-load the parallel data 1101 as in (3), above; keep the same settings as in (4a) *except* set the right serial input data switch to HIGH and again pulse the clock six times. Again record and screen shot the Q_A - Q_D outputs at the start and after each pulse and discuss the differences from 4(a).

(c) Push the clear button, Again record and screen shot the Q_A - Q_D outputs discuss the results

(d) From the end result of step (c), and with the mode switches still set for shift right, again pulse the clock but now alternate the right serial input switch between high and low for each pulse, for at least 8 pulses. Again record and screen shot the Q_A - Q_D outputs at the start and after each pulse

In your report explain the results, drawing a chart showing how the data progresses through the internal registers.

(5) Shift Left Serial Output for the '194

(a) Load 1101 into the register as in (3), above, set the mode to shift left (S_1=high, S_0=low), and set the left serial input to LOW. Pulse the clock input six times. Record and screen shot the Q_A - Q_D outputs at the start and after each pulse.

(b) Re-load the parallel data 1101 as in (3), above; keep the same settings as (5a) *except* set the left serial input data switch to HIGH and again pulse the clock six times. Again record and screen shot the Q_A - Q_D outputs at the start and after each pulse and discuss the differences from 5(a).

In your report explain the results, drawing a chart showing how the data progresses through the internal registers.

(6) Serial to Parallel output with the '194

(a) Push the clear button and confirm that the registers are cleared.

(b) Set the mode to shift right (S_1=low, S_0=high), and set the right serial input to HIGH. Pulse the clock input once. Set the right serial input to LOW. Pulse the clock input once. Set the right serial input to HIGH. Pulse the clock input once. Set the right serial input to HIGH. Pulse the clock input once. Record and screen shot the Q_A - Q_D outputs at the start and after each pulse. What digital word has been loaded into the register and is now on the outputs?

(7) Recirculating Data with the '194

(a) Construct a recirculating shift register by disconnecting the right input from the data-switch and connecting it instead to the Q_D output as shown in figure 2, below (which does not show the other necessary connections).

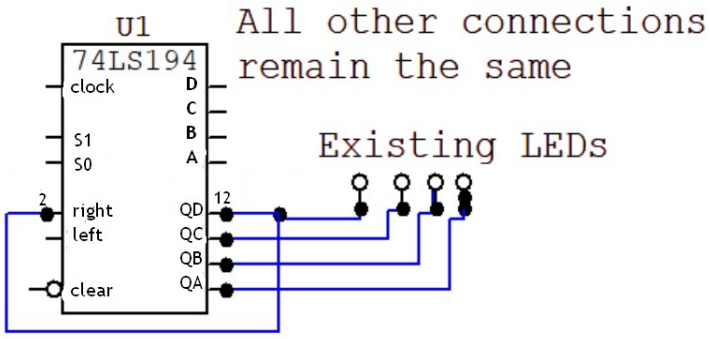

Figure 2. recirculating Modification

(b) Load 1101 into the register as in (3), above

(c) Set the mode to shift right (S_1=low, S_0=high)

(d) pulse the clock at least 10 times. Record and screen shot the Q_A - Q_D outputs at the start and after each pulse.

In your report explain the results, drawing a chart showing how the data progresses through the internal registers.

FAIRCHILD SEMICONDUCTOR™

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DM74LS194A
4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load

Shift right (in the direction Q_A toward Q_D)

Shift left (in the direction Q_D toward Q_A)

Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is HIGH and S1 is LOW. Serial data for this mode is entered at the shift-right data input. When S0 is LOW and S1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

Features

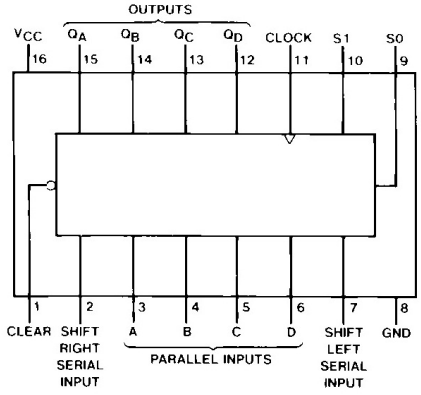
- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

Ordering Code:

Order Number	Package Number	Package Description
DM74LS194AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS194AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

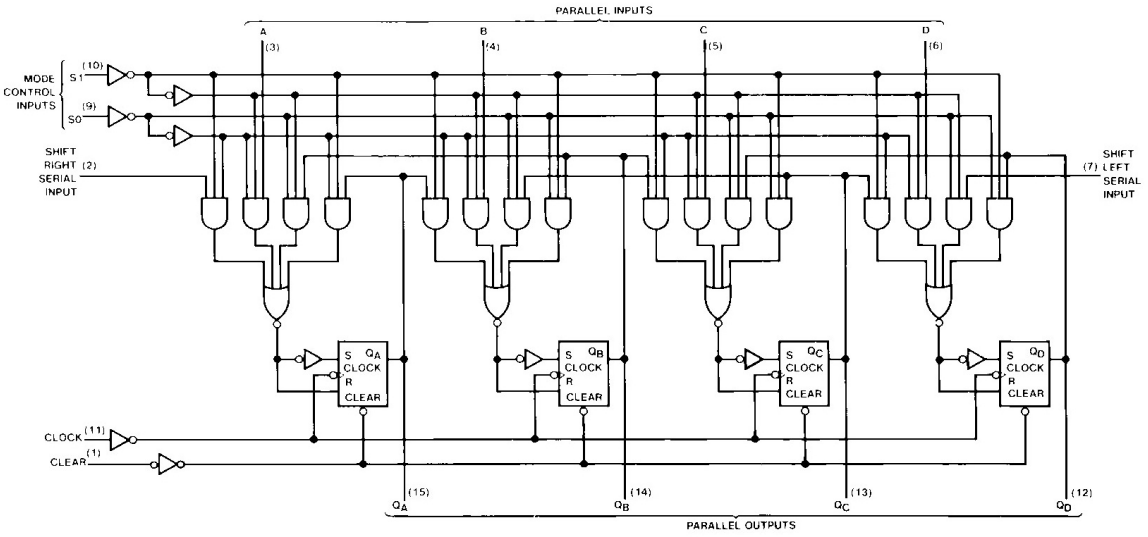


Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Logic Diagram



Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	C_L = 50 pF, R_L = 2 kΩ		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		26	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Clear to Any Q		38	ns

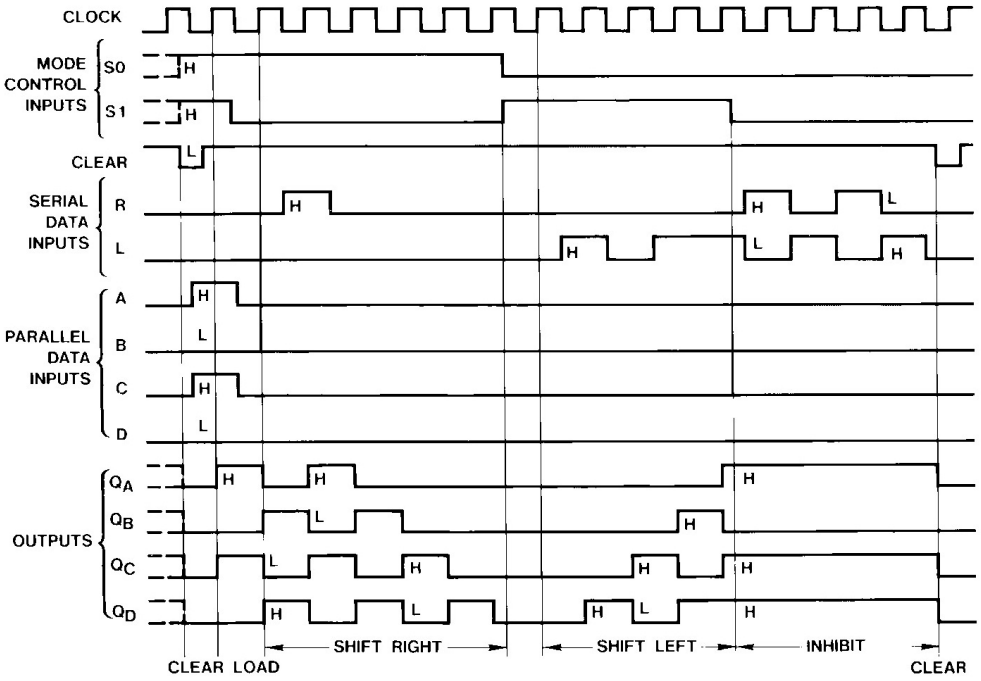
Note 8: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 10: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)