EQUIPMENT NEEDED:

Analog Discovery
Computer with Waveform program
7400, quad 2-input NAND
7473, JK M-S Flip-flop

Notes:

1) **Before** wiring each circuit you must have a neat logic diagram showing pin numbers used and functional interconnections. (All circuit diagrams must be included in your report.) When actually assembling the circuit make sure you are using the proper IC. Also do not forget to hook up power and ground to each IC you use and indicate pin numbers for this.
2) For ease of typing, negation is sometimes indicated by an asterisk, apostrophe or tilde. Thus $\overline{X}$ is the same as X*, which is the same as X', and which is the same as ~X; which are all ways of writing not X (or active low X).

A. The $\overline{S}$-$\overline{R}$ Latch

Connect two sections of a 7400 2-input NAND gate as shown in figure 1, below, using two of the virtual data switches as inputs and two of the virtual LEDs as output indicators.

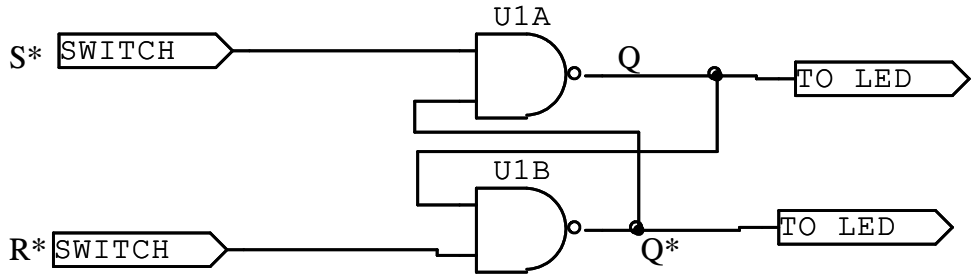


Figure 1, S*-R* Latch

(1) Set inputs S*=1 and R*=1 (high). Record the state of the outputs.

(2) Momentarily bring the S* input to 0 for a brief time (switch its data switch to 0 and set it back to 1 again). Record the state of the outputs after you pulse the inputs like this.

(3) Leaving the S* input high, momentarily bring the R* input to 0 for a brief time (switch its data switch to 0 and set it back to 1 again). Record the state of the outputs after you pulse the inputs like this.

(4) Put both input switches into the 0 (low) position and leave them there. Record the state of the outputs; is this a valid condition or not? Explain why in your report.

(5) First return S* to 1 and then R* to 1. Record the state of the outputs.

(6) Again set S*=0 and R*=0. Then first return R* to 1, and then S* to 1. Record the state of the outputs

(7) From the results of this section complete the truth table for the S*-R* Latch. A suggested format is shown in figure 2, below

INPUTS		OUTPUTS		
R*	S*	Q	Q*	Comments
0	0			
0	1			
1	0			
1	1			

Figure 2, Suggested format of final truth table for S*-R* Latch

B. Gated S-R Latch.

Construct a gated latch using 4 sections of the 7400 chip as shown in figure 3, below.

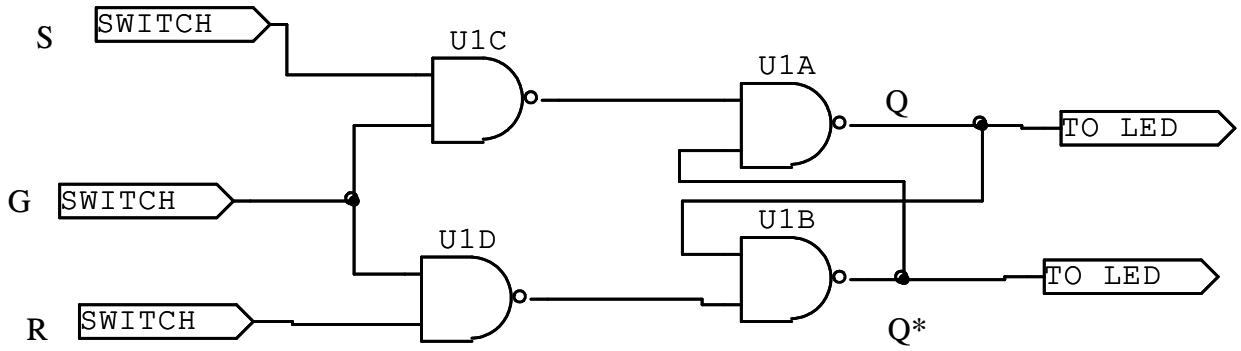


Figure 3, Gated R-S Latch

Develop the truth table for this latch by doing the following steps in sequence, recording the state of the outputs for each step. (Start with the gate input G=0, which should disable all inputs.)

(1) Set R=1, S=1; leave G=0
(2) Set R=1, S=0; leave G=0
(3) Set R=0, S=0; leave G=0
(4) Set R=0, S=1; leave G=0

Note: in steps 1-4 the latch should have remained in the same state. Explain why in your report. Was the particular state you observed the same for all groups in the lab? (Check with other students.) Explain why in your report.

(5) Set the gate input G=1, which should enable all inputs
Set S=1, R=0; leave G=1
(6) Set S=0, R=0; leave G=1
(7) Set S=0, R=1; leave G=1
(8) with G=1, Set S=1, R=1; then set G=0 record the outputs for each state of G
In your report explain the operation of the latch for step 8.

In your report complete the truth table for the Gated S-R latch. A suggested format is shown in figure 4, below.

INPUTS			OUTPUTS		
G	R	S	Q	Q*	Comments
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Figure 4, Suggested format of final truth table for Gated S-R Latch.

C. JK Master-Slave (M-S) Flip Flop, 7473.

(1) Wire the 7473 as shown in figure 5 using virtual switches and virtual LEDs and a virtual push button output (BUTTON: 0 to 1) on the Analog Discovery as the clock input. Do not forget to hook up, and indicate on your diagram, 5V power and ground (note they are NOT pins 7 and 14).

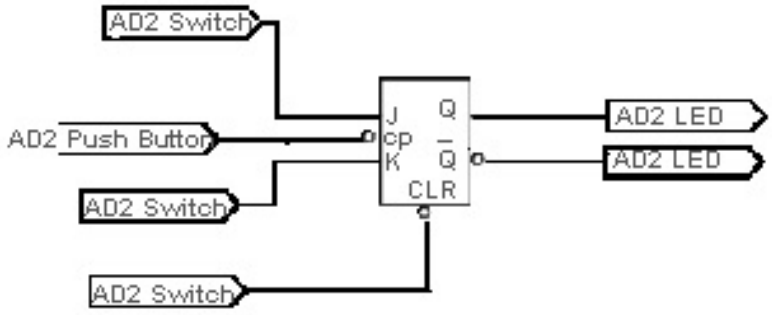


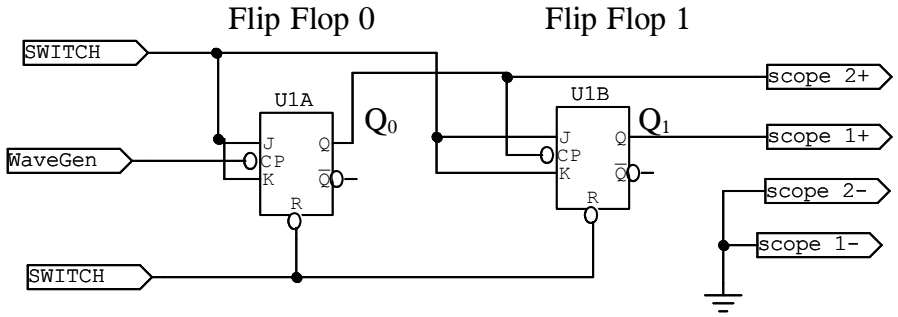
Figure 5, Connections to 7473

(2) Verify the synchronous (clocked) truth table for the 7473 (see data sheet) as well as verifying that no change will occur on the outputs, even if the inputs are changed, unless the complete clock signal is present (a transition from low-to-high and back to low). Record the state of the outputs clearly in truth table format similar to the table in the data sheet.

(3) Verify the asynchronous operation of the 7473 by bring the direct clear (or reset) input low. Verify that it will remain reset, with the clear input overriding all possible conditions at J, K, & CK. Record how you did this.

D. Interconnected Flip-Flops; Dynamic Operation -- Asynchronus

(1) Interconnect the two halves of the 7473 as shown in figure 6, below.



Other Connections:
Vcc (pin __)
gnd (pin__)

Figure 6, Asynchronous Binary Counter

(2) Set the virtual data switches so that the clear input is HIGH and the J and K inputs are also high. Use the Analog Discovery WaveGen to provide a positive 0 to 5V square wave of 100KHz frequency to the clock input instead of a push button. Be sure to reset the default settings of this virtual instrument. You need a peak-to-peak amplitude of 5V, so set the amplitude (which is peak) to be 2.5V. Set the offset to +2.5V so the signal will be 0 to 5V.

Take a "screen shot" of the set-up of the static I/O and the WaveGen and include it in your report. In your report be sure you clearly indicate the meaning of each relevant switch and LED either by labeling the I/O in the Analog Discovery or by indicating the static I/O numbers on your wiring diagram.

(3) Put the Q_0 and Q_1 outputs into the two signal inputs 2+ and 1+ of the Analog Discovery virtual 'scope and trigger the 'scope on the negative-going transition of the Q_1 output of flip-flop 1. Set a trigger level well into the expected amplitude of the outputs, you can try +1V. Offset the two traces so that the Q_1 output is on the top half of the screen and the Q_0 on the bottom.

Run the set-up and observe the waveforms on the 'scope. Take a screen shot of the 'scope (preferred) or draw the timing diagram showing these waveforms for at least 8 clock cycles (adjust the sec/div setting for this). Include this timing diagram in your report – it is part of your data for this section. In your report state the frequency of the Q_0 and Q_1 outputs and the value of the input frequency. What is the ratio of the input frequency to each of the outputs?

(4) Set the clear input LOW and continue to observe and record the outputs. What effect did this have on the operation of the counter?

(5) Set the clear input back to HIGH, then set the J and K inputs LOW and continue to observe and record the outputs. What effect did this have on the operation of the counter?

(6) In your report, **for each of the counters in D, E, and F**, starting with the counter state $Q_1=1$, $Q_2=1$, list the consecutive counter states for at least the next 7 clock pulses. Note that a table

such as shown in figure 7, listing consecutive states, is called a "State-Table." Comment on the type of the counter for each state-table you make up, *eg*: what modulo, up or down, etc.

Pulse	Q_1	Q_0	
0	1	1	
1			
2			
3			
4			
5			
6			
7			
8			

Figure 7, Sample State-Table

(7) Before disconnecting the counter, have the instructor look at your set-up and sign your data sheet or wiring diagram.

E. Truncated count:

(1) Before disconnecting your asynchronous counter add a decoder to the circuit so it is a modulo 3 instead of modulo 4 counter. One way of doing the is a simple NAND gate with the inputs connected to Q_1 and Q_0 and the output connected to both R* inputs of the 7473 instead of the switch. See figure 8, below.

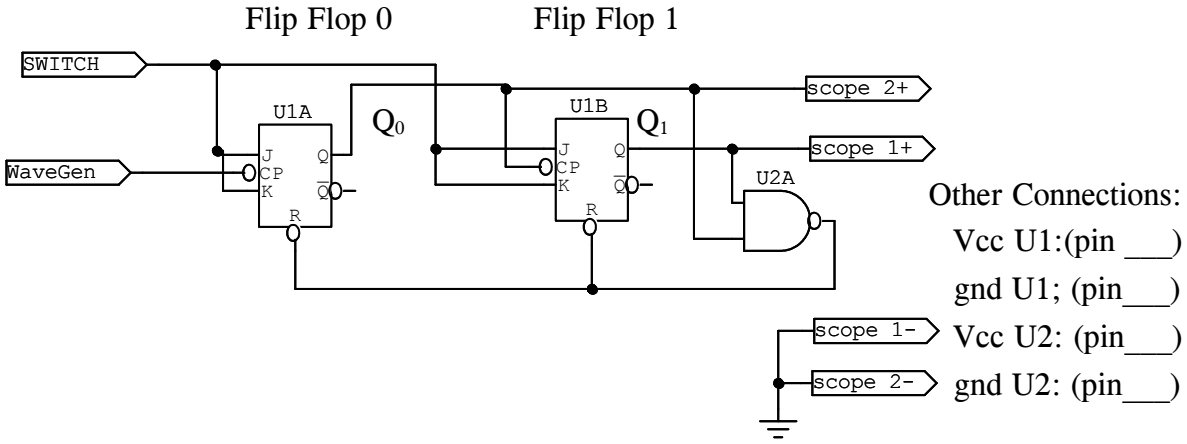


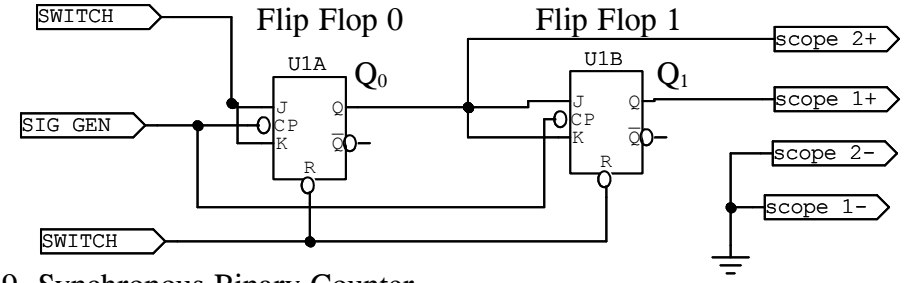
Figure 8, Suggested Truncated Asynchronous Binary Counter

Repeat steps (2). (3). (6), and (7) from part D, above.

F. Interconnected Flip-Flops; Dynamic Operation -- Synchronous

(1) Construct the circuit shown in figure 9, on next page. This is a synchronous binary counter because the clocks in all the circuits receive their signals simultaneously.

Repeat steps (2) through (7) from part D, above.



Other Connections:

V_{cc}(pin __)

gnd; (pin__)

Figure 9, Synchronous Binary Counter

11/27/17-dw

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised February 2000

DM7473
Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

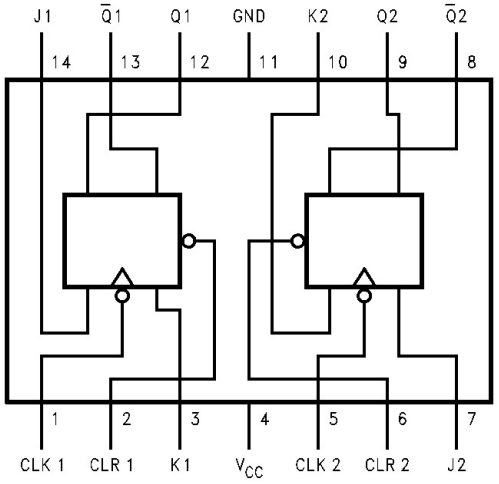
General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is LOW the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is HIGH the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is HIGH. Data transfers to the outputs on the falling edge of the clock pulse. A LOW logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM7473N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

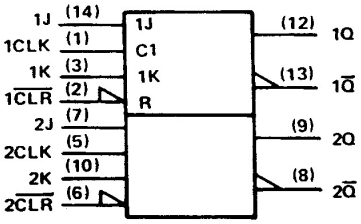
H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
⎍ = Positive pulse data. the J and K inputs must be held constant while the clock is HIGH. Data is transferred to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each HIGH level clock pulse.

‘73, SN54LS73A, SN7473, SN74LS73A
_ J-K FLIP-FLOPS WITH CLEAR

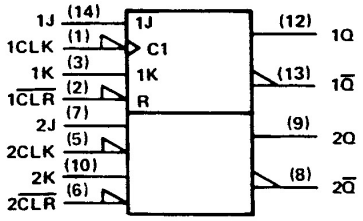
– DECEMBER 1983 – REVISED MARCH 1988

symbols†

‘73



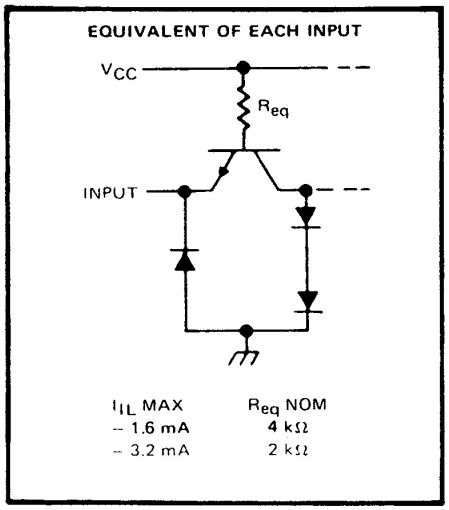
‘LS73A

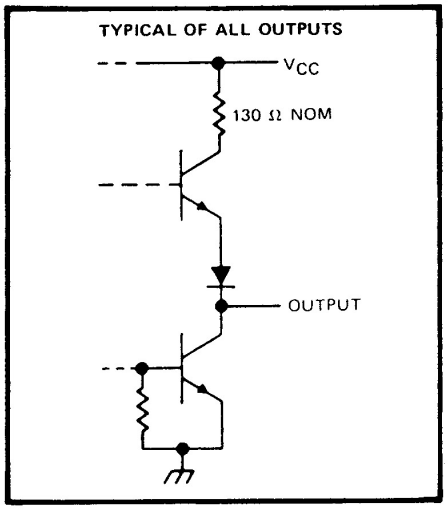


† symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

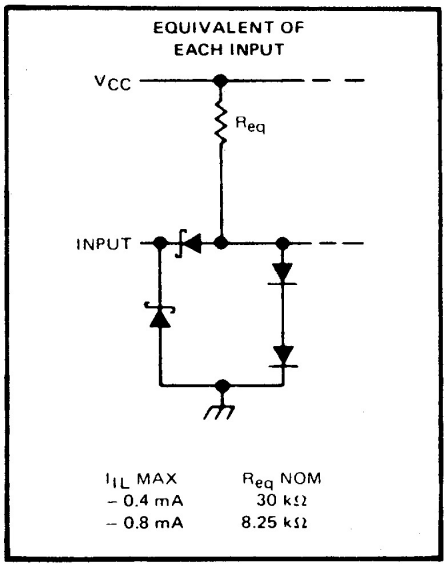
ıatics of inputs and outputs

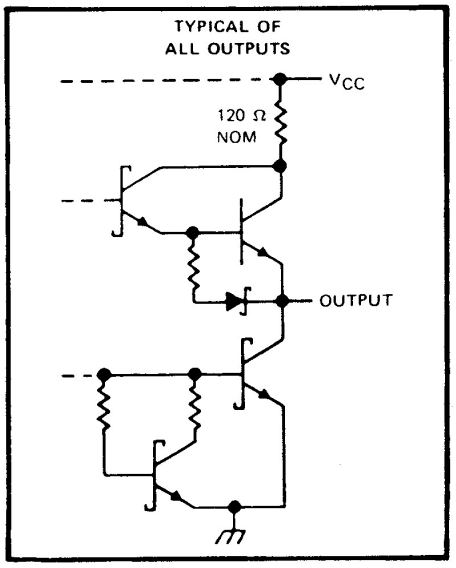
‘73





‘LS73





Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 3)		0		15	MHz
t_W	Pulse Width (Note 3)	Clock HIGH	20			ns
		Clock LOW	47			
		Clear LOW	25			
t_{SU}	Input Setup Time (Note 2)(Note 3)		0↑			ns
t_H	Input Hold Time (Note 2)(Note 3)		0↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -12$ mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = Min$, $I_{OH} = Max$, $V_{IL} = Max$, $V_{IH} = Min$		2.4	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$, $V_{IH} = Min$, $V_{IL} = Max$			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = Max$, $V_I = 5.5V$				1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = Max$, $V_I = 2.4V$	J, K			40	µA
			Clock			80	
			Clear			80	
I_{IL}	LOW Level Input Current	$V_{CC} = Max$, $V_I = 0.4V$	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	$V_{CC} = Max$ (Note 5)		−18		−55	mA
I_{CC}	Supply Current	$V_{CC} = Max$, (Note 6)			18	34	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time.

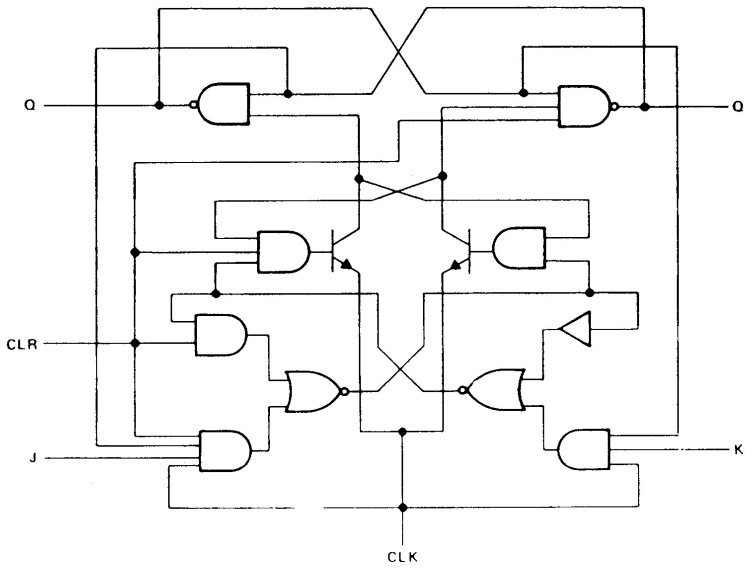
Note 6: With all outputs OPEN, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn. At the time of measurement the clock input grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

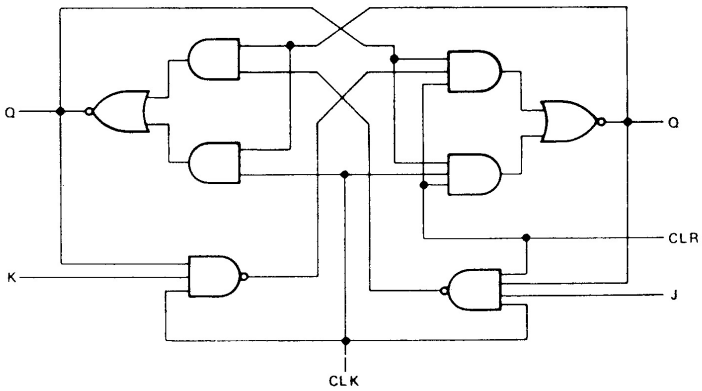
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

logic diagrams (positive logic)

'73



'LS73A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage: '73 . . . . . 5.5 V
'LS73A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0° C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.