ELT-217, **Experiment AD-4x**: ADDERS

OBJECTIVE:
To investigate the performance of Adder Circuits both using individual gates and an MSI IC.

EQUIPMENT NEEDED:

2 ea. - 7400 Quad NAND IC
1 ea. - 7486 Quad XOR IC
1 ea. - 74LS283 4-bit adder IC
Analog Discovery
Computer
breadboard and wire as needed

GENERAL:

Before actually wiring, make a schematic diagram showing which virtual switch and/or virtual LED is connected to what; show all connections and pin numbers. **It is strongly recommended that you arrange all switches and LEDs so that they are in order, on the same line, with the MSB at the left and LSB on the right.** Include clearly labeled diagrams in your report for each different set-up.

PROCEDURE:

Part 1 Using individual gates.

Construct an adder able to add two 2-bit numbers from a half-adder and a full adder built using only XOR and NAND gates. Your test book should show a logic diagram for this 2-bit adder. In your report explain clearly the logic functions occurring and why this has the proper function. Use Three of your virtual LED's to observe the outputs and four virtual data switches to control the inputs. Include in your report a complete wiring diagram, including pin numbers and AD2 connections.

The adder should be able to add two 2-bit binary numbers, A and B, consisting of A_1A_0 & B_1B_0 to get a 3-bit sum consisting of Sum_1, Sum_0, and the carry C_{OUT}. In other words:

$$\begin{array}{rr} & A_1\ A_0 \\ +\ & B_1\ B_0 \\ \hline C_{OUT} & Sum_1\ Sum_0 \end{array}$$

Verify that your adder is working properly by testing all 16 possible input combinations of numbers A & B. Also show a block diagram in your report of how you could connect half and/or full adders (as blocks) to add one four-bit number to another four-bit number. Figure out how many gates you would need to actually implement your block diagram.

Take a “screen shot” of any one set of data and include it in your report. In your report be sure you clearly indicate which set of data is being tested and the meaning of each relevant switch and LED.

Part 2 Using a single MSI I.C.,

Use the 74LS283 adder to construct an adder capable of working with two 4-bit binary numbers. Show the wiring diagram clearly in your report. Use eight virtual switches for the data inputs (A_1-A_4 and B_1-B_4). Use one additional virtual switch for the carry in (C_0). Use five virtual LEDs to show the states of the four Sum Outputs ($\sum_1$ - $\sum_4$) and the Carry Output (C_4). It is suggested that all the I/O channels chosen be arranged on your screen so that they are in normal significant bit order with the MSB at the left and the LSB at the right.

Verify the positive-logic addition operation of the 74LS283 for the binary equivalent of the following sets of decimal data:

a) 4 + 3, Carry in=0

b) 4 + 3, Carry in=1

c) 12 + 3, Carry in=1

d) 8 + 7, Carry in=0

e) 9 + 12, Carry in=0

f) 11 + 3, Carry in=1

g) other data as assigned by the instructor

Take a "screen shot" of any one set of data and include it in your report. In your report clearly indicate what set of data is being tested and the meaning of each switch and LED.

In your report comment on the differences in using a more versatile MSI chip in place of wiring individual gates.

11/3/19 – dw

MOTOROLA

SN54/74LS283

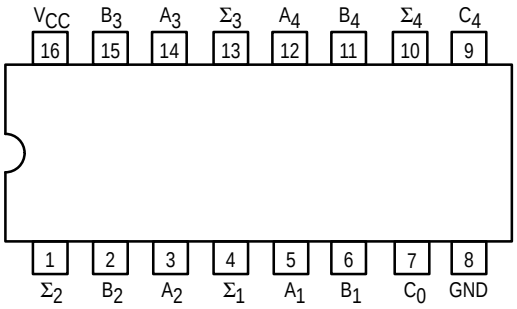
4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

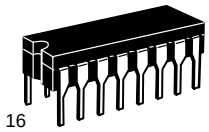
4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY

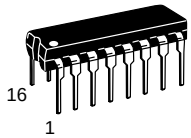
CONNECTION DIAGRAM DIP (TOP VIEW)



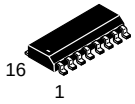
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

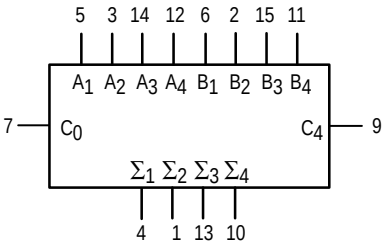
		LOADING (Note a) HIGH	LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

ORDERING INFORMATION

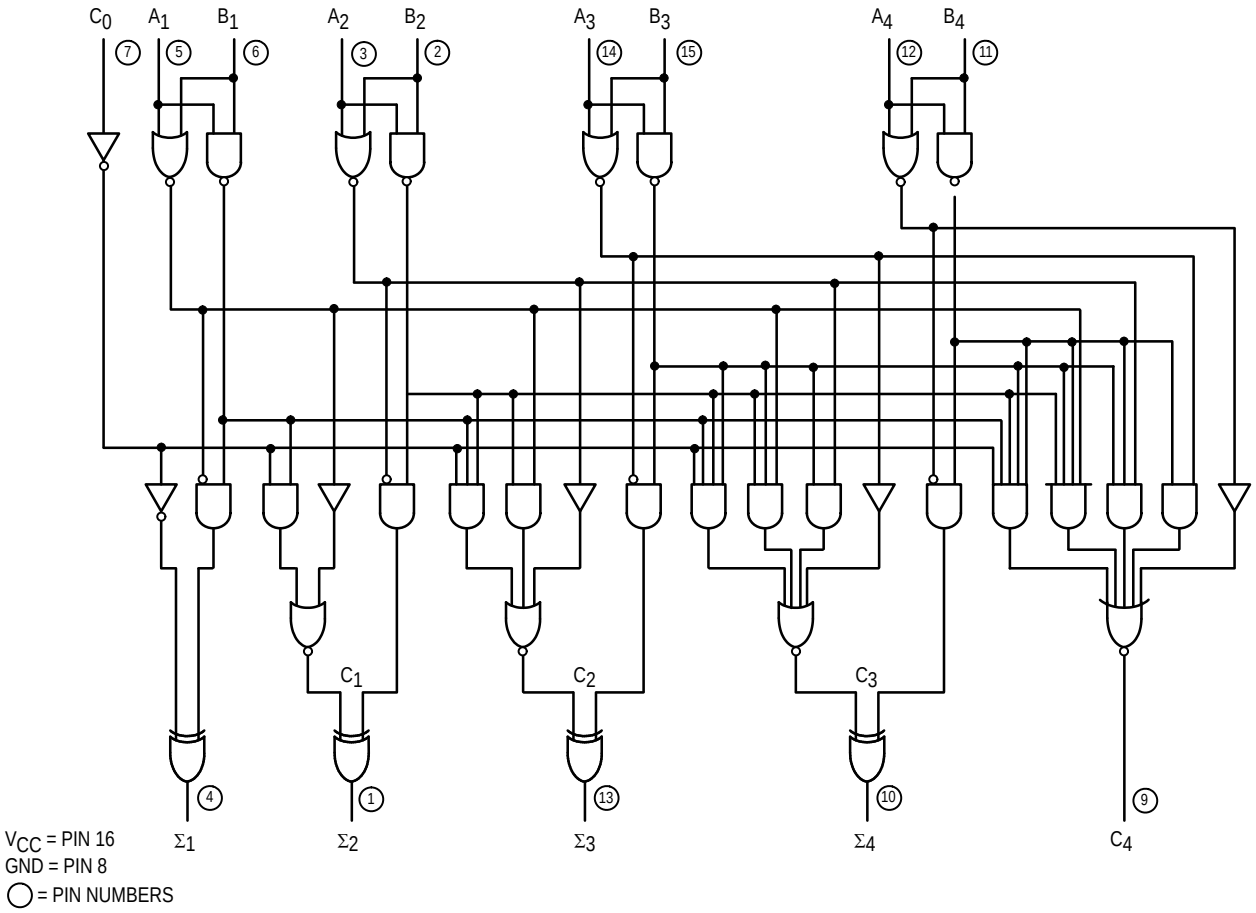
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C4) outputs.

$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 7, 5 or 3.

FUNCTIONAL TRUTH TABLE

C (n−1)	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

$C_1 - C_3$ are generated internally
C_0 is an external input
C_4 is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	C_0			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		Any A or B			40	μA		
		C_0			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		Any A or B			0.2	mA		
I_{IL}	Input LOW Current	C_0			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Any A or B			−0.8	mA		
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				34	mA	V_{CC} = MAX	
	Total, Output LOW				39			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to Any Σ Output		16 15	24 24	ns	C_L = 15 pF Figures 1 & 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 11	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

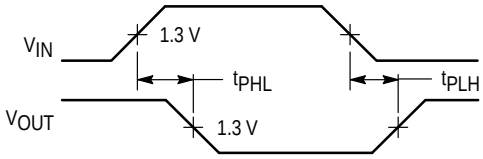


Figure 1

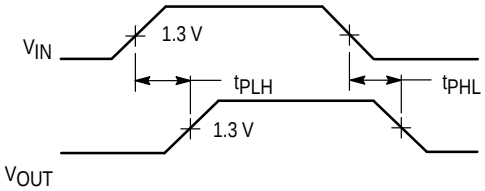


Figure 2