**Flip-flops/latches/registers**

Ascychronus inputs take presidence -and changes happen with them

All other changes happen only with the clock --level; rising edge; or falling edge

**S-R** not clocked – depends on input levels

S=R=0 --hold; S=1, R=0 – Q=1 (set) ; S=0, R=1 – Q=0 (reset)

**Gated S-R**

If gate = active, acts like an S-R

If gate = inactive, – holds – and s-r inputs have no effect

**D- Output follows the input**

for transparent latches, if enable is active output follows input if it changes; if enable = inactive. holds

for edge triggered latches, input immediately before edge is held after the edge has past

**J-K**

J and K control the clocked changes

J=K=0 – no change; J=1, K=0 –Q=1 (set); J=0, K=1 – Q=0 (reset) ; J=K=1 Q= Q0\* (toggles)

may have preset (set) and/or clear (reset) asynchronous inputs

Ripple Counters

* clock is fed into first (LSB) FF
* output of one FF is fed into the clock of the next FF
* number of states (mod) = 2n where n= number of FFs
* can have less than 2n states if you reset before end
* usually has master set and/or reset asynchronously

Synchronus Counters

* all clocks are connected together
* what each J-K FF does is controlled by either toggling (J=K=1) or holding (J=K=0) depending on the previous count-- logic may be required
  + Q0=LSB ,, J=K=1
  + Q1=next bit, J=K=Q0
  + Q2=next bit, J=K= (Q0=1 & Q1=1)
* number of states (mod) = 2n where n= number of FFs
* can have less than 2n states if you reset before end
* usually has master set and/or reset asynchronously
* may have a load function

IC’s

Know what the function of the circuit is and analize overall function

* may have Enable which lets the whole circuit works
* usually has master set and/or reset asynchronously
* may have a load function \_
* may have a function control input, for example “U/D\*” or “U/D” which would mean “up” when high and “down”when low