Disable: To disallow or deactivate a function or circuit.

Enable: To allow or activate a function or circuit.

Fault: The problem in a nonfunctioning electrical circuit. It is usually due to an open circuit, short circuit, or defective component.

Float: A logic level in a digital circuit that is neither HIGH nor LOW. It acts like an open circuit to anything connected to it.

Gate: The basic building block of digital electronics. The basic logic gate has one or more inputs and one output and is used to perform one of the following logic functions: AND, OR, NOR, NAND, INVERT, exclusive-OR, or exclusive-NOR.

Hex: When dealing with integrated circuits, a term specifying *six* gates on a single IC package.

Inversion Bar: A line over variables in a Boolean equation signifying that the digital state of the variables is to be complemented. For example, the output of a two-input NAND gate is written $X = \overline{AB}$.

Johnson Shift Counter: A digital circuit that produces several repetitive digital waveforms useful for specialized waveform generation.

Logic Probe: An electronic tool used in the troubleshooting procedure to indicate a HIGH, LOW, or float level at a particular point in a circuit.

Logic Pulser: An electronic tool used in the troubleshooting procedure to inject a pulse or pulses into a particular point in a circuit.

NOT: When reading a Boolean equation, the word used to signify an inversion bar. For example, the equation $X = \overline{AB}$ is read "X equals NOT AB."

Quad: When dealing with integrated circuits, the term specifying *four* gates on a single IC package.

Repetitive Waveform: A waveform that repeats itself after each cycle.

Troubleshooting: The work that is done to find the problem in a faulty electrical circuit.

Truth Table: A tabular listing that is used to illustrate all the possible combinations of digital input levels to a gate and the output that will result.

Waveform Generator: A circuit used to produce specialized digital waveforms.

Problems

Section 3–1

3–1. Build the truth table for:

(a) a three-input AND gate.

(b) a four-input AND gate.

3–2. If we were to build a truth table for an eight-input AND gate, how many different combinations of inputs would we have?

3–3. Describe in words the operation of:

(a) an AND gate.

(b) an OR gate.

Section 3–2

3–4. Determine the logic level at *W*, *X*, *Y* and *Z* in Figure P3–4.

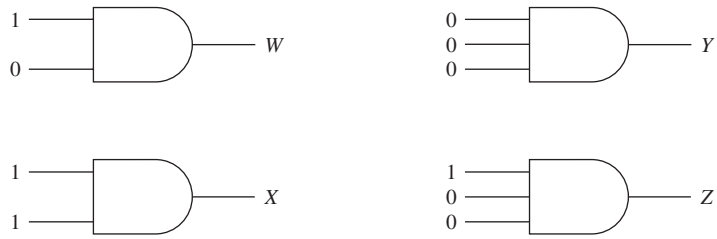

Figure P3–4

3–5. Write the Boolean equation for

(a) A three-input AND gate

(b) A four-input AND gate

(c) A three-input OR gate

3–6. Determine the logic level at *W*, *X*, *Y* and *Z* in Figure P3–6.

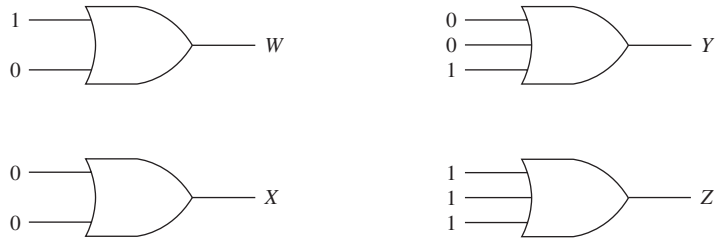

Figure P3–6

Section 3–3

3–7. Sketch the output waveform at *X* for the two-input AND gates shown in Figure P3–7.

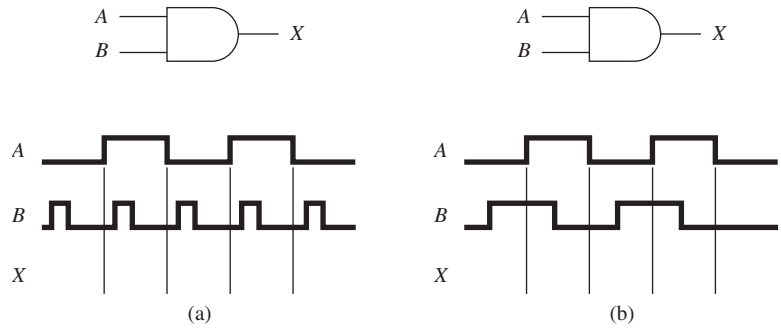

Figure P3–7

3–8. Sketch the output waveform at *X* for the two-input OR gates shown in Figure P3–8.

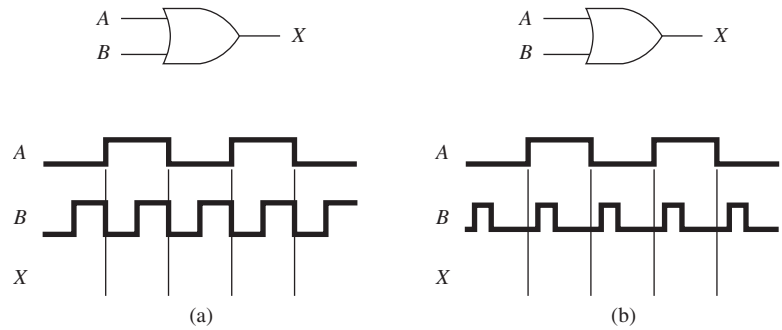

Figure P3–8

3–9. Sketch the output waveform at *X* for the three-input AND gates shown in Figure P3–9.

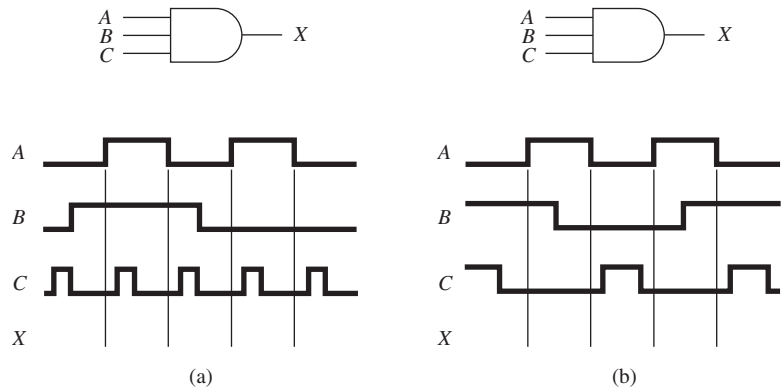

Figure P3–9

C **3–10.** The input waveform at *A* is given for the two-input AND gates shown in Figure P3–10. Sketch the input waveform at *B* that will produce the output at *X*.

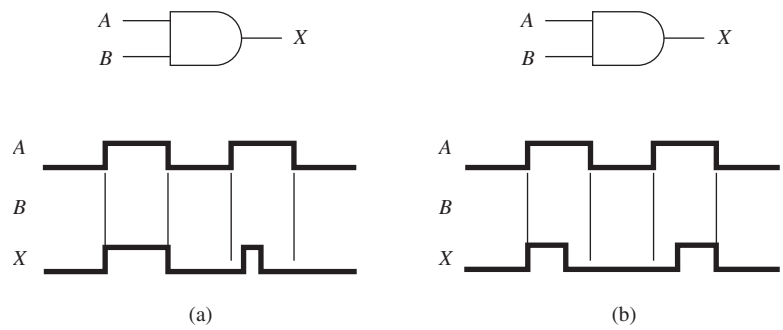

Figure P3–10

C **3–11.** Repeat Problem 3–10 for the two-input OR gates shown in Figure P3–11.

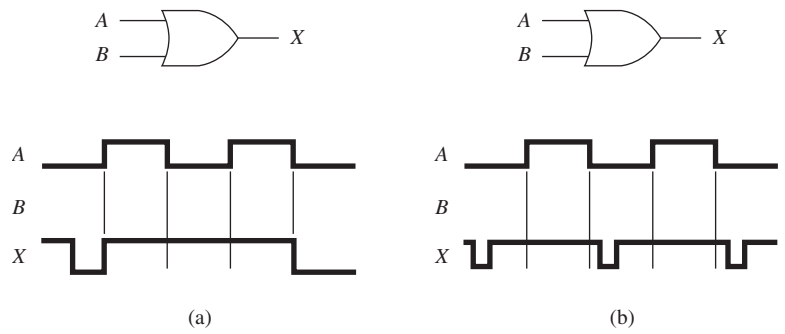

Figure P3–11

Section 3–4

3–12. Using Figure P3–12, sketch the waveform for the *enable signal* that will allow pulses 2, 3 and 6, 7 to get through to the receiving device.

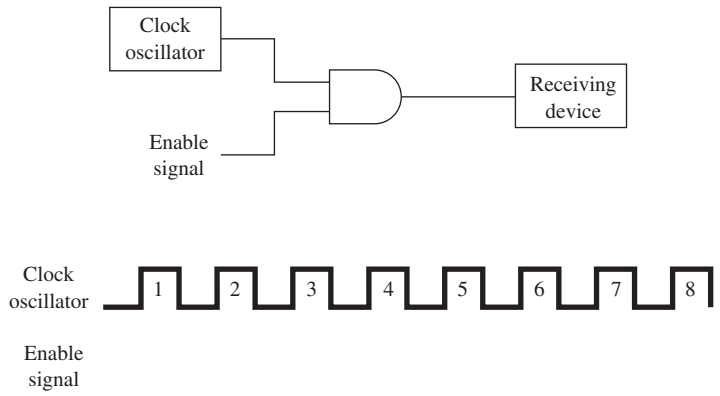

Figure P3–12

3–13. Repeat Problem 3–12, but this time sketch the waveform that will allow only the even pulses (2, 4, 6, 8) to get through.

Section 3–5

3–14. How many separate OR gates are contained within the 7432 TTL IC?

3–15. Sketch the actual pin connections to a 7432 quad two-input OR TTL IC to implement the circuit of Figure 3–18.

3–16. How many inputs are there on each AND gate of a 7421 TTL IC?

3–17. The 7421 IC is a 14-pin DIP. How many of the pins are *not* used for anything?

Section 3–6

T* **3–18.** What are the three logic levels that can be indicated by a logic probe?

T **3–19.** What is the function of the logic pulser?

*The letter **T** designates a problem that involves **T**roubleshooting.

T **3–20.** When troubleshooting an OR gate such as the 7432, when the pulser is applied to one input, should the other input be connected HIGH or LOW? Why?

T **3–21.** When troubleshooting an AND gate such as the 7408, when the pulser is connected to one input, should the other input be connected HIGH or LOW? Why?

C T **3–22.** The clock enable circuit shown in Figure P3–22 is not working. The enable switch is up in the enable position. A logic probe is placed on the following pins and gets the following results. Find the cause of the problem.

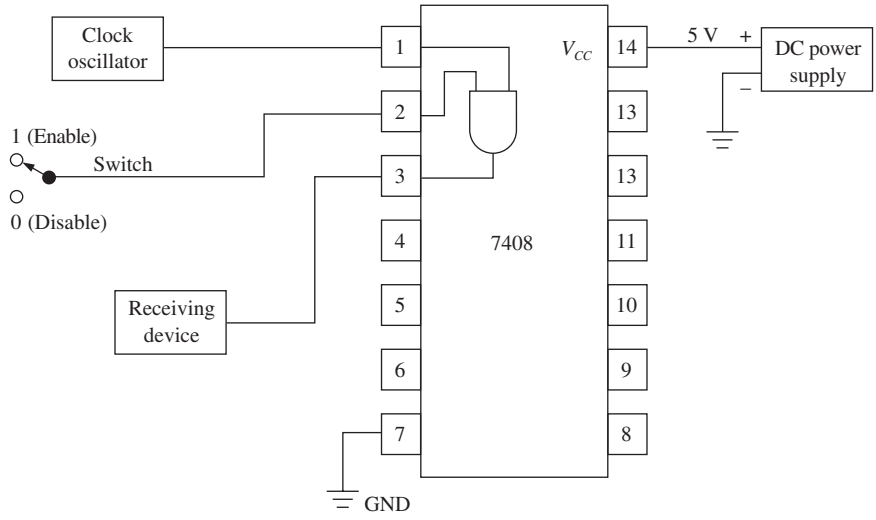

Figure P3–22

Probe on Pin	Indicator Lamp
1	Flashing
2	On
3	Off
7	Off
14	On

C T **3–23.** Repeat Problem 3–22 for the following troubleshooting results.

Probe on Pin	Indicator Lamp
1	Flashing
2	Off
3	Off
7	Off
14	On

C T **3–24.** Repeat Problem 3–22 for the following troubleshooting results.

Probe on Pin	Indicator Lamp
1	Flashing
2	On
3	Off
7	Dim
14	On

Section 3–7

3–25. For Figure P3–25, write the Boolean equation at X. If $A = 1$, what is X?

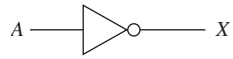

Figure P3–25

3–26. For Figure P3–26, write the Boolean equation at X and Z. If $A = 0$, what is X? What is Z?

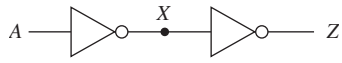

Figure P3–26

3–27. Using Figure P3–26, sketch the output waveform at X and Z if the timing waveform shown in Figure P3–27 is input at A.

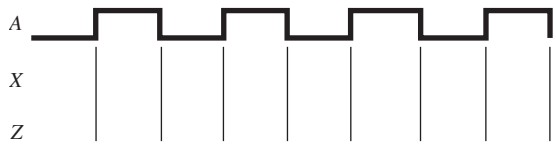

Figure P3–27

Section 3–8

3–28. For Figure P3–28, write the Boolean equation at X and Y and build a truth table for each.

Figure P3–28

3–29. Determine the logic levels at W, X, Y and Z in Figure P3–29.

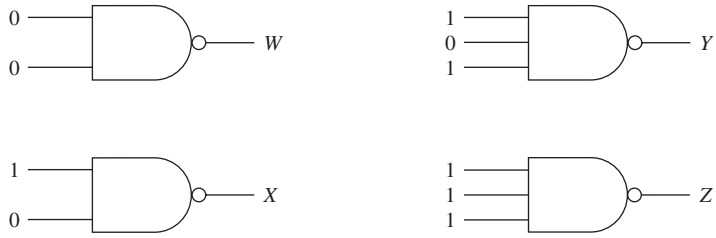

Figure P3–29

3–30. Using Figure P3–28, sketch the output waveforms for X and Y, given the input waveforms shown in Figure P3–30. ($X = \overline{AB}$, $Y = \overline{CD}$)

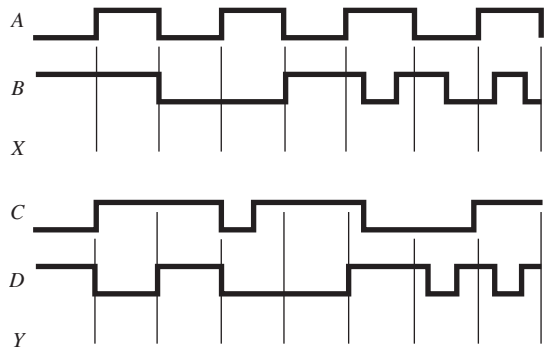

Figure P3–30

Section 3–9

3–31. Determine the logic level at *W*, *X*, *Y* and *Z* in Figure P3–31.

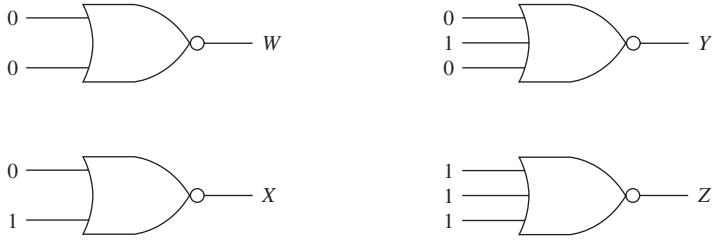

Figure P3–31

3–32. Using Figure P3–32, sketch the waveforms at *X* and *Y* with the switches in the down (0) position. Repeat with the switches in the up (1) position.

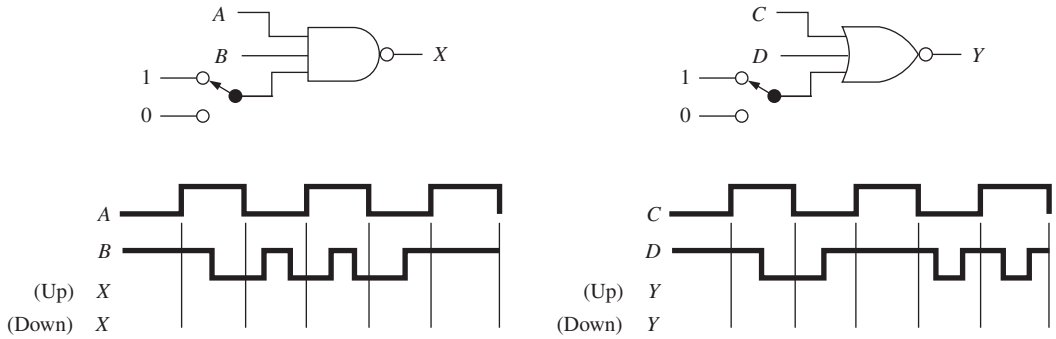

Figure P3–32

3–33. In words, what effect does the switch have on each circuit in Figure P3–32?

3–34. For Figure P3–34, write the Boolean equation at *X* and *Y* and build a truth table for each.

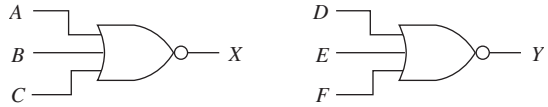

Figure P3–34