## Problems

### Section 5–1

**5–1.** Write the Boolean equation for each of the logic circuits shown in Figure P5–1.

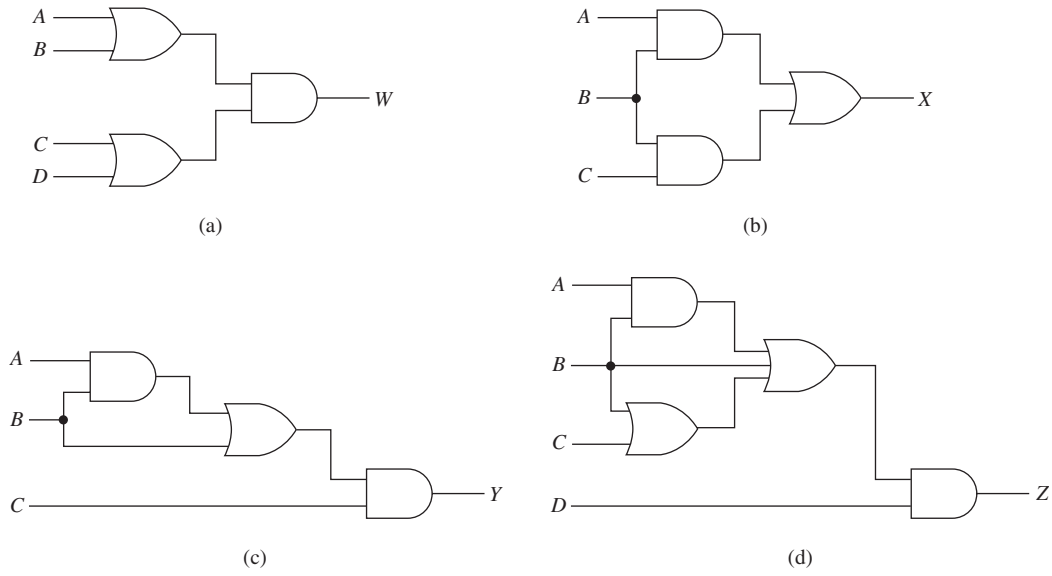



**Figure P5–1**

**5–2.** Refer to the gray water reclamation tank in Figure 5–7 (Example 5–4). Write the Boolean equation and draw the logic circuit to implement the following functions:

**(a)** Turn on the red light ($R$) if there is a HIGH opacity ($C$) and pressure ($P$) when the level is full ($F$).

**(b)** Turn on the green light ($G$) if there is a HIGH opacity ($C$) and pressure ($P$) when the level is mid ($M$) or full ($F$).

**(c)** Turn on the blue light ($B$) when the tank level is full and any of the sensors for PH ($H$), opacity ($C$), or pressure ($P$) are HIGH.

### Section 5–2

**5–3.** Draw the logic circuit that would be used to implement the following Boolean equations. Also, construct a truth table for each of the equations. (*Hint:* Where applicable, apply Law 3 to the equation first. *Do not* simplify the equation for this problem.)

**(a)** $M = (AB) + (C + D)$

**(b)** $N = (A + B + C)D$

**(c)** $P = (AC + BC)(A + C)$

**(d)** $Q = (A + B)BCD$

**(e)** $R = BC + D + AD$

**(f)** $S = B(A + C) + AC + D$

**5–4.** Write the Boolean equation and then complete the timing diagram at *W*, *X*, *Y*, and *Z* for the logic circuits shown in Figure P5–4.

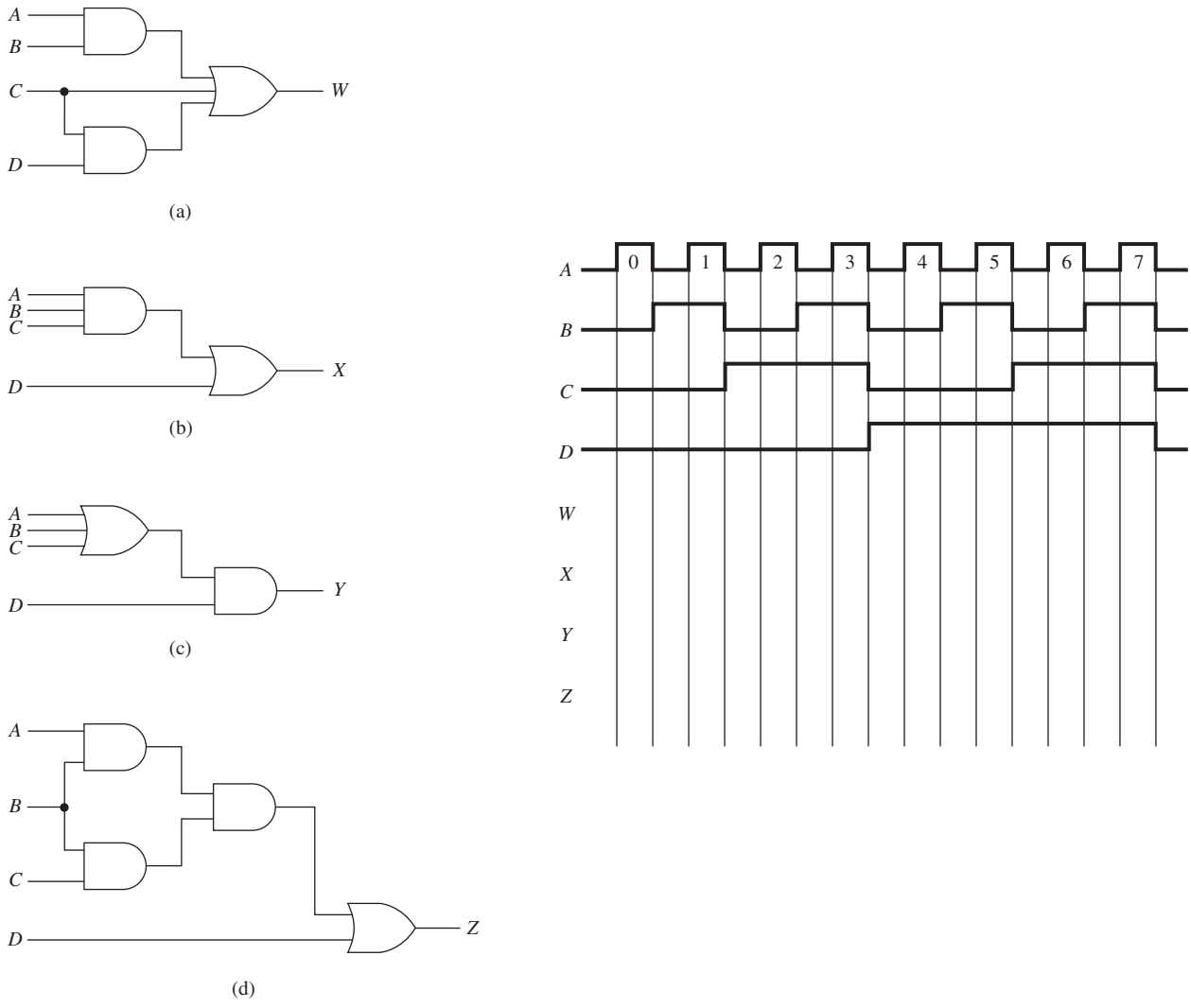
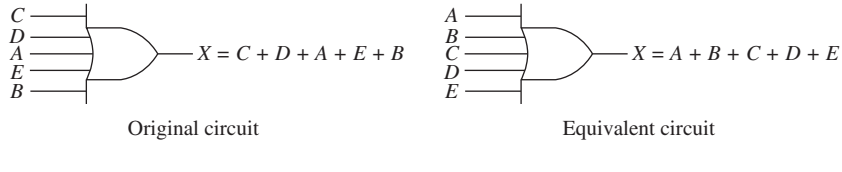



**Figure P5–4**

**5–5.** State the Boolean law that makes each of the equivalent circuits shown in Figure P5–5 valid.




(a)

**Figure P5–5**

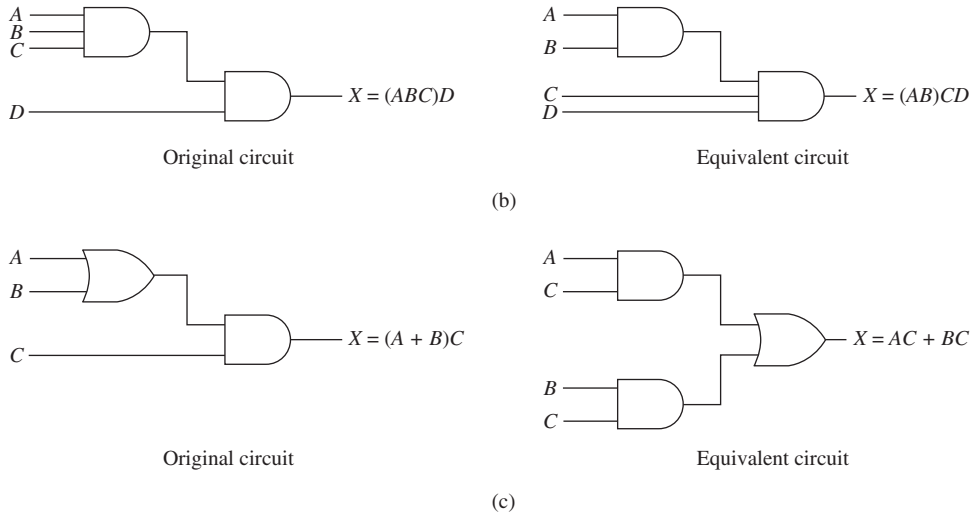



**Figure P5–5** *Continued*

**5–6.** Using the 10 Boolean rules presented in Table 5–2, determine the outputs of the logic circuits shown in Figure P5–6.

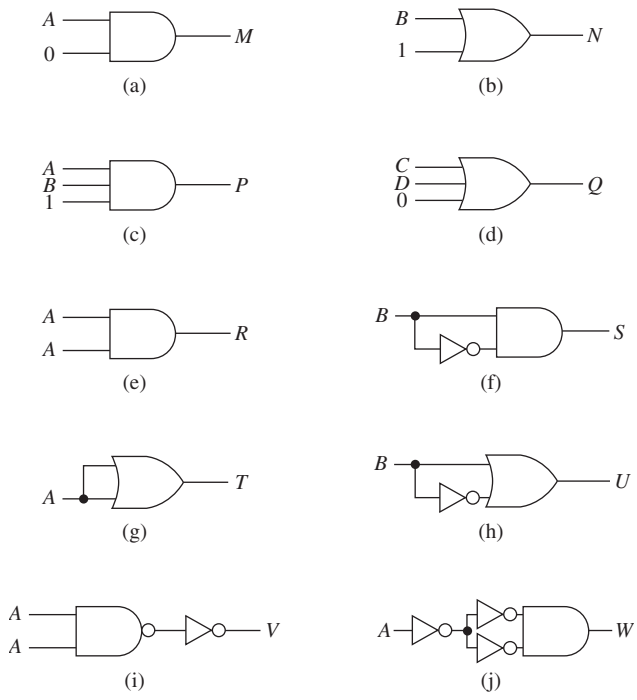



**Figure P5–6**

## Section 5–3

**5–7.** Write the Boolean equation for the circuits of Figure P5–7. Simplify the equations, and draw the simplified logic circuit.

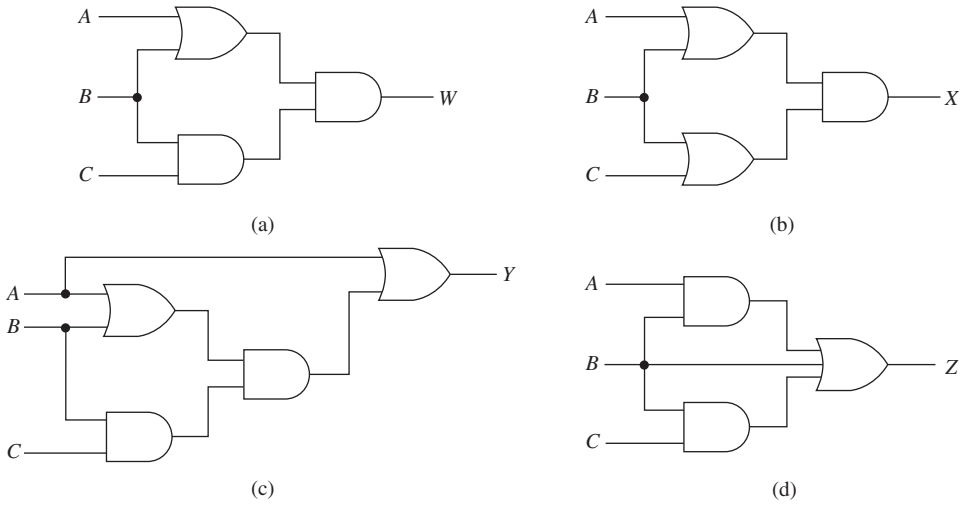



**Figure P5–7**

**5–8.** Repeat Problem 5–7 for the circuits shown in Figure P5–8.

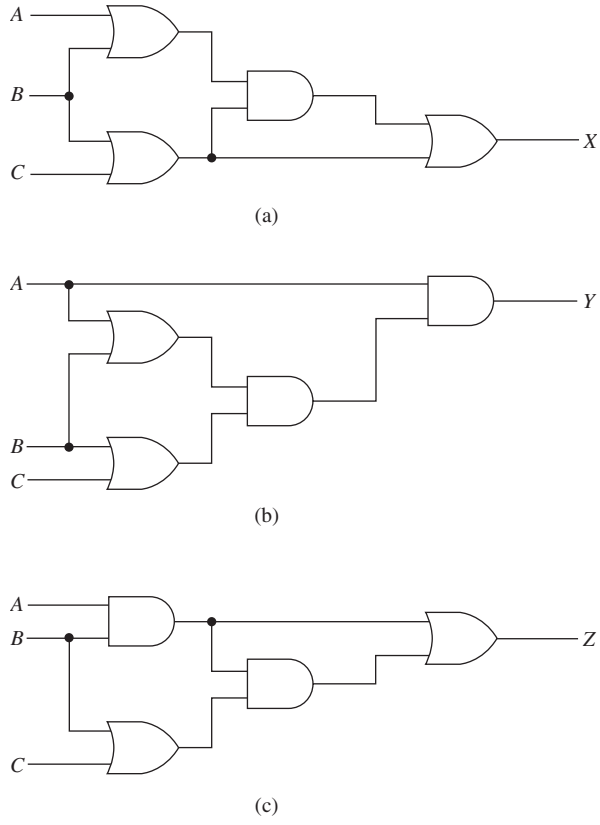



**Figure P5–8**

**5–9.** Draw the logic circuit for the following equations. Simplify the equations, and draw the simplified logic circuit.

**(a)** $V = AC + ACD + CD$

**(b)** $W = (BCD + C)CD$

**(c)** $X = (B + D)(A + C) + ABD$

**(d)** $Y = AB + BC + ABC$

**(e)** $Z = ABC + CD + CDE$

**5–10.** Construct a truth table for each of the simplified equations of Problem 5–9.

**5–11.** The pin layouts for a 74HCT08 CMOS AND gate and a 74HCT32 CMOS OR gate are given in Figure P5–11. Make the external connections to the chips to implement the following logic equation. (Simplify the logic equation first.)

$$X = (A + B)(D + C) + ABD$$

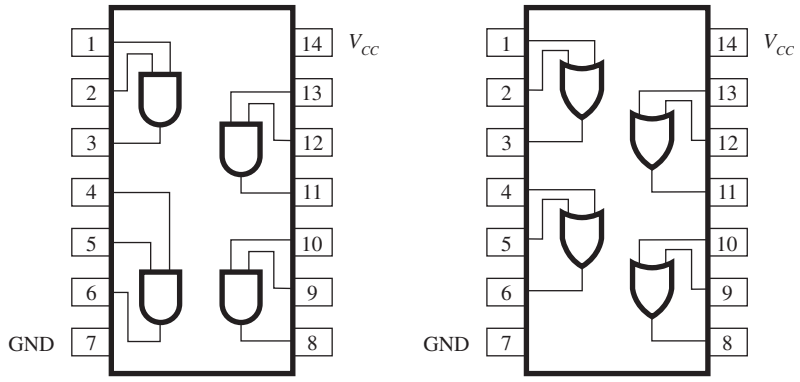



**Figure P5–11**

**5–12.** Repeat Problem 5–11 for the following equation

$$Y = AB(C + BD) + BD$$

## Section 5–5

**5–13.** Write a sentence describing how De Morgan's theorem is applied in the simplification of a logic equation.

**5–14.** **(a)** De Morgan's theorem can be used to prove that an OR gate with inverted inputs is equivalent to what type of gate?

**(b)** An AND gate with inverted inputs is equivalent to what type of gate?

**5–15.** Which two circuits in Figure P5–15 produce equivalent output equations?

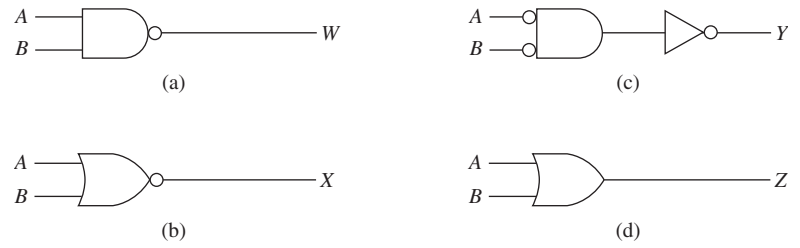



**Figure P5–15**

**5–16.** Use De Morgan's theorem to prove that a NOR gate with inverted inputs is equivalent to an AND gate.

**5–17.** Draw the logic circuit for the following equations. Apply De Morgan's theorem and Boolean algebra rules to reduce them to equations having inversion bars over single variables only. Draw the simplified circuit.

**(a)** $W = \overline{AB} + \overline{A + C}$

**(b)** $X = A\overline{B + C} + \overline{BC}$

**(c)** $Y = \overline{(AB) + C} + B\overline{C}$

**(d)** $Z = \overline{AB + (\overline{A} + C)}$

**5–18.** Write the Boolean equation for the circuits of Figure P5–18. Use De Morgan's theorem and Boolean algebra rules to simplify the equation. Draw the simplified circuit.

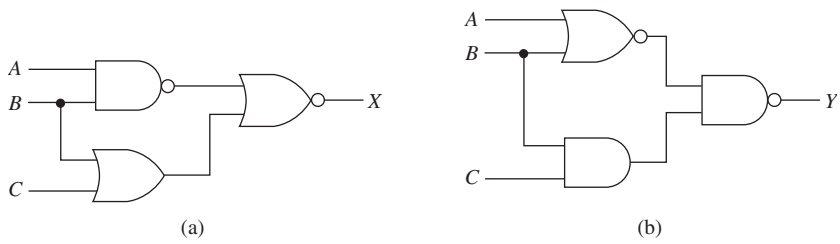



**Figure P5–18**

C **5–19.** Repeat Problem 5–17 for the following equations.

**(a)** $W = \overline{\overline{AB} + CD} + \overline{AC\overline{D}}$

**(b)** $X = \overline{\overline{A} + B \cdot BC} + \overline{B}C$

**(c)** $Y = \overline{AB\overline{C} + D} + \overline{A\overline{B} + B\overline{C}}$

**(d)** $Z = (C + D)\overline{A\overline{C}D}(\overline{A}C + \overline{D})$

C **5–20.** Repeat Problem 5–18 for the circuits of Figure P5–20.

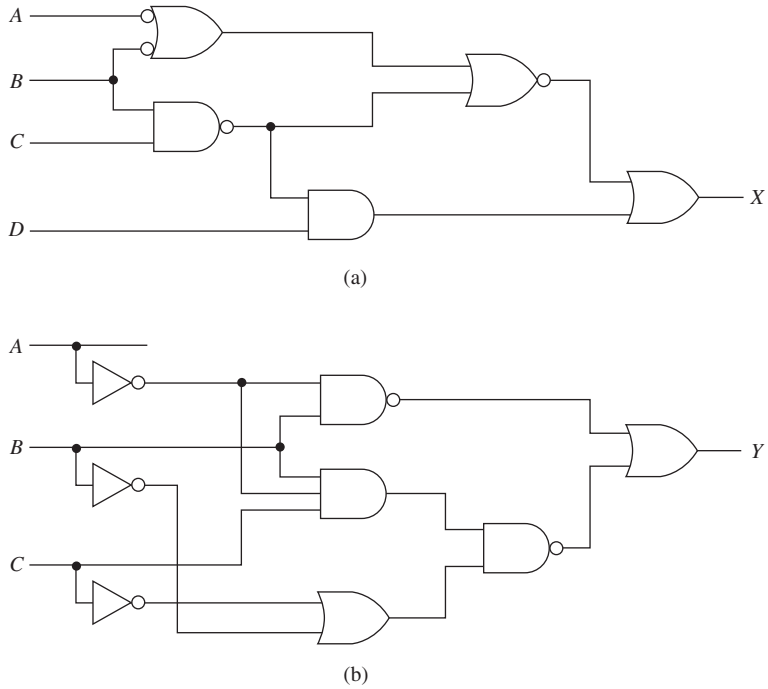



**Figure P5–20**

D* **5–21.** Design a logic circuit that will output a 1 (HIGH) only if $A$ and $B$ are both 1 while either $C$ or $D$ is 1.

D **5–22.** Design a logic circuit that will output a 0 only if $A$ or $B$ is 0.

D **5–23.** Design a logic circuit that will output a LOW only if $A$ is HIGH or $B$ is HIGH while $C$ is LOW or $D$ is LOW.

C D **5–24.** Design a logic circuit that will output a HIGH if only one of the inputs $A$, $B$, or $C$ is LOW.

C D **5–25.** Design a circuit that outputs a 1 when the binary value of $ABCD$ ($D$ = LSB) is $> 11$.

C D **5–26.** Design a circuit that outputs a LOW when the binary value of $ABCD$ ($D$ = LSB) is $> 7$ and $< 10$.

**5–27.** Complete a truth table for the following simplified Boolean equations.

**(a)** $W = A\overline{B}\,\overline{C} + \overline{B}C + \overline{A}B$

**(b)** $X = \overline{A}\,\overline{B} + A\overline{B}C + B\overline{C}$

**(c)** $Y = \overline{C}D + \overline{A}\,B\,\overline{C}\,\overline{D} + BCD + \overline{A}C\overline{D}$

**(d)** $Z = \overline{A}BC\overline{D} + \overline{A}C + C\overline{D} + \overline{B}\,\overline{C}$

**5–28.** Complete the timing diagram in Figure P5–28 for the following simplified Boolean equations.

**(a)** $X = \overline{A}\,\overline{B}\,\overline{C} + ABC + A\overline{C}$

**(b)** $Y = \overline{B} + \overline{A}B\overline{C} + AC$

**(c)** $Z = B\overline{C} + A\overline{B} + \overline{A}BC$

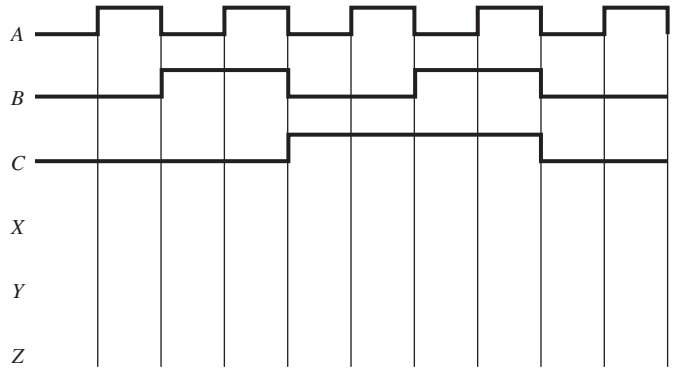



Figure P5–28

**5–29.** Use the bubble-pushing technique to convert the gates in Figure P5–29.

*The letter D designates a circuit D esign problem.

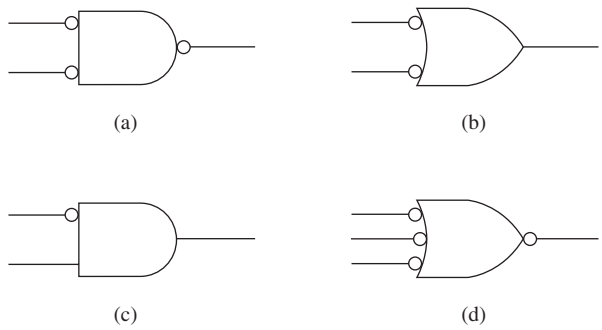



**Figure P5–29**

D C **5–30.** Some computer systems have two disk drives, commonly called drive A and drive B, for storing and retrieving data. Assume that your computer has four control signals provided by its internal microprocessor to enable data to be read and written to either drive. Design a gating scheme similar to that provided in Figure 5–60 to supply an active-LOW drive select signal to drive A ($\overline{DS_a}$) or to drive B ($\overline{DS_b}$) whenever they are read or written to. The four control signals are also active-LOW and are labeled $\overline{RD}$ (Read), $\overline{WR}$ (Write), $\overline{DA}$ (drive A), and $\overline{DB}$ (drive B).

## Section 5–7

**5–31.** Draw the connections required to convert

**(a)** A NAND gate into an inverter

**(b)** A NOR gate into an inverter

**5–32.** Draw the connections required to construct

**(a)** An OR gate from two NOR gates

**(b)** An AND gate from two NAND gates

**(c)** An AND gate from several NOR gates

**(d)** A NOR gate from several NAND gates

**5–33.** Redraw the logic circuits of Figure P5–33 to their equivalents *using only* NOR gates.

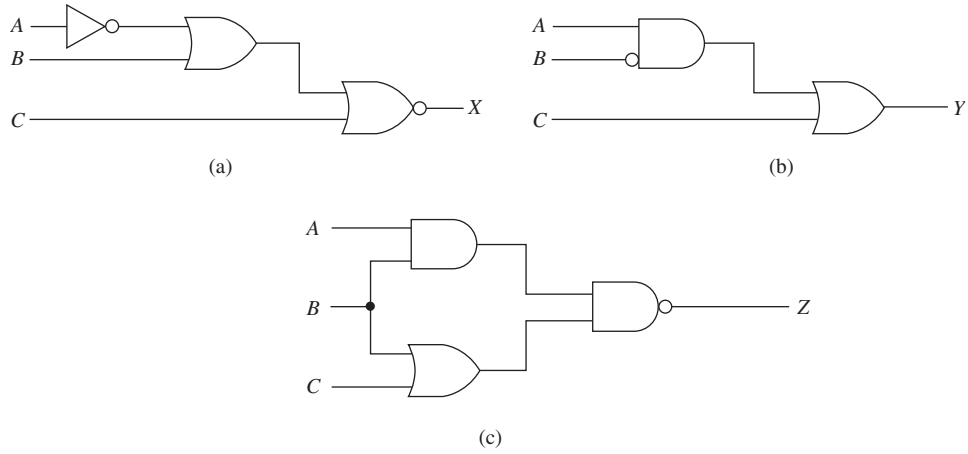



**Figure P5–33**

C

**5–34.** Convert the circuits of Figure P5–34 to their equivalents *using only* NAND gates. Next, make the external connections to a 7400 quad NAND to implement the new circuit. (Each new equivalent circuit is limited to *four* NAND gates.)

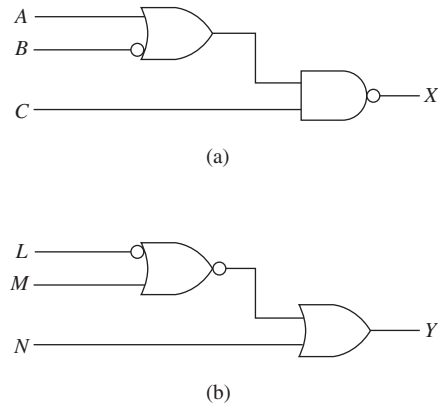



**Figure P5–34**

## Section 5–8

**5–35.** Identify each of the following Boolean equations as a POS expression, a SOP expression, or both.

**(a)** $U = A\overline{B}C + BC + \overline{A}C$

**(b)** $V = (A + C)(\overline{B} + \overline{C})$

**(c)** $W = A\overline{C}(\overline{B} + C)$

**(d)** $X = AB + \overline{C} + BD$

**(e)** $Y = (A\overline{B} + D)(A + \overline{C}D)$

**(f)** $Z = (A + \overline{B})(BC + A) + \overline{A}B + CD$

**5–36.** Simplify the circuit of Figure P5–36 down to its SOP form, then draw the logic circuit of the simplified from implemented using a 74LS54 AOI gate.

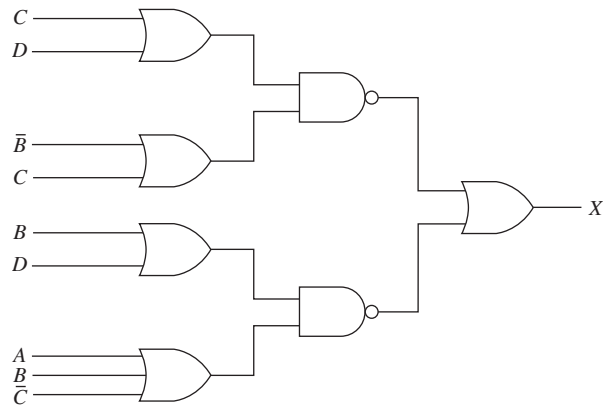



**Figure P5–36**

## Section 5–9

**5–37.** Using a Karnaugh map, reduce the following equations to a minimum form.

**(a)** $X = AB\overline{C} + \overline{A}B + \overline{A}\,\overline{B}$

**(b)** $Y = BC + \overline{A}\,\overline{B}C + B\overline{C}$

**(c)** $Z = ABC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + AB\overline{C}$

**5–38.** Using a Karnaugh map, reduce the following equations to a minimum form.

**(a)** $W = \overline{B}(C\overline{D} + \overline{A}D) + \overline{B}\,\overline{C}(A + \overline{A}\,\overline{D})$

**(b)** $X = \overline{A}\,\overline{B}\,\overline{D} + B(\overline{C}\,\overline{D} + ACD) + A\overline{B}\,\overline{D}$

**(c)** $Y = A(C\overline{D} + \overline{C}\,\overline{D}) + A\overline{B}D + \overline{A}\,\overline{B}C\overline{D}$

**(d)** $Z = \overline{B}\,\overline{C}D + B\overline{C}D + \overline{C}\,\overline{D} + C\overline{D}(B + \overline{A}\,\overline{B})$

C **5–39.** Use a Karnaugh map to simplify the circuits in Figure P5–39.

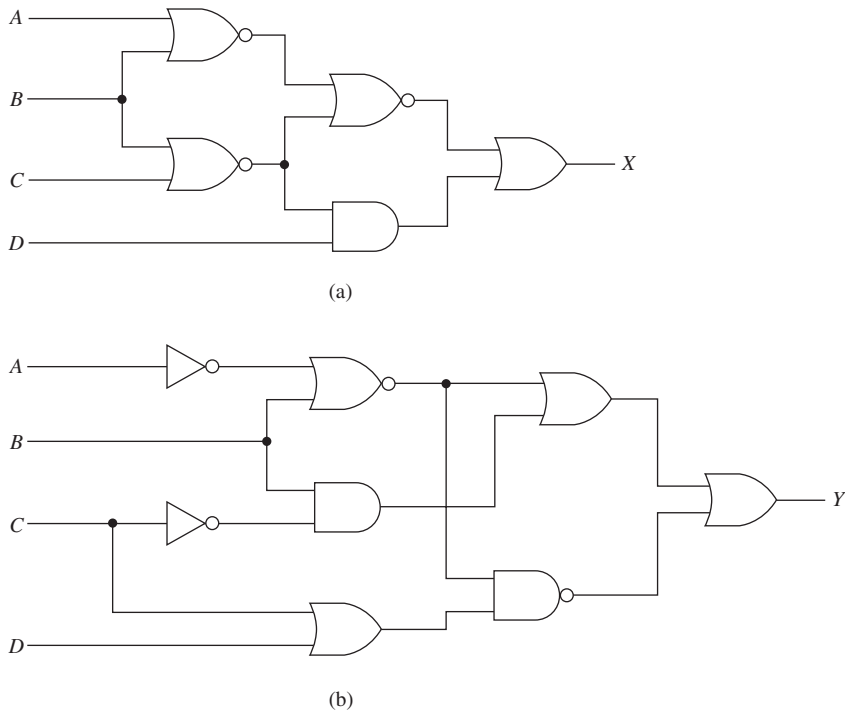



**Figure P5–39**

## Section 5–10

C **5–40.** Seven-segment displays are commonly used in calculators to display each decimal digit. Each segment of a digit is controlled separately, and when all seven of the segments are on, the number 8 is displayed. The upper right segment of the display comes on when displaying the numbers 0, 1, 2, 3, 4, 7, 8, and 9. (The numerical designation for each of the digits 0 to 9 is shown in Figure P5–40 and described in more detail in Section 12–6.) Design a circuit that outputs a HIGH (1) whenever a 4-bit BCD code translates to a number that uses the upper right segment. Use variable $A$ to represent the $2^3$ BCD input. Implement your design with an AOI and inverters.

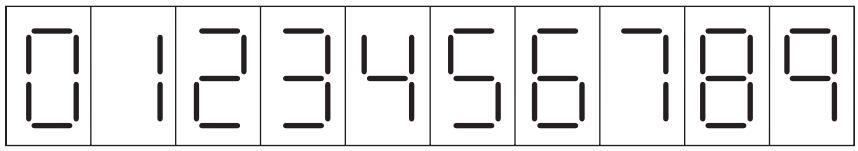
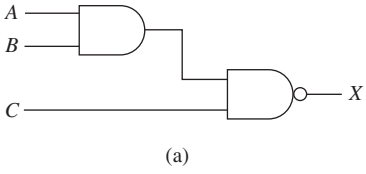


Figure P5–40

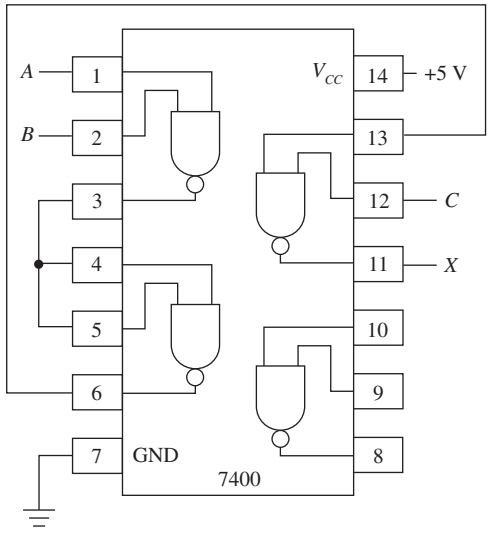
C D **5–41.** Repeat Problem 5–40 for the lower left segment of a seven-segment display (0, 2, 6, 8).

T **5–42.** The logic circuit of Figure P5–42(a) is implemented by making connections to the 7400 as shown in Figure P5–42(b). The circuit is not working properly. The problem is in the IC connections or in the IC itself. The data table in Figure P5–42(c) is completed by using a logic probe at each pin. Identify the problem.




(a)

Test conditions
$A = 1$
$B = 1$
$C = 1$
$X$ should equal 0




(b)

| Probe on pin: | Indicator lamp |
|---|---|
| 1 | On |
| 2 | On |
| 3 | Off |
| 4 | Off |
| 5 | Off |
| 6 | Off |
| 7 | Off |
| 8 | On |
| 9 | Dim |
| 10 | Dim |
| 11 | On |
| 12 | On |
| 13 | Off |
| 14 | On |

(c)

Figure P5–42

T **5–43.** Repeat Problem 5–42 for the circuit shown in Figure P5–43.

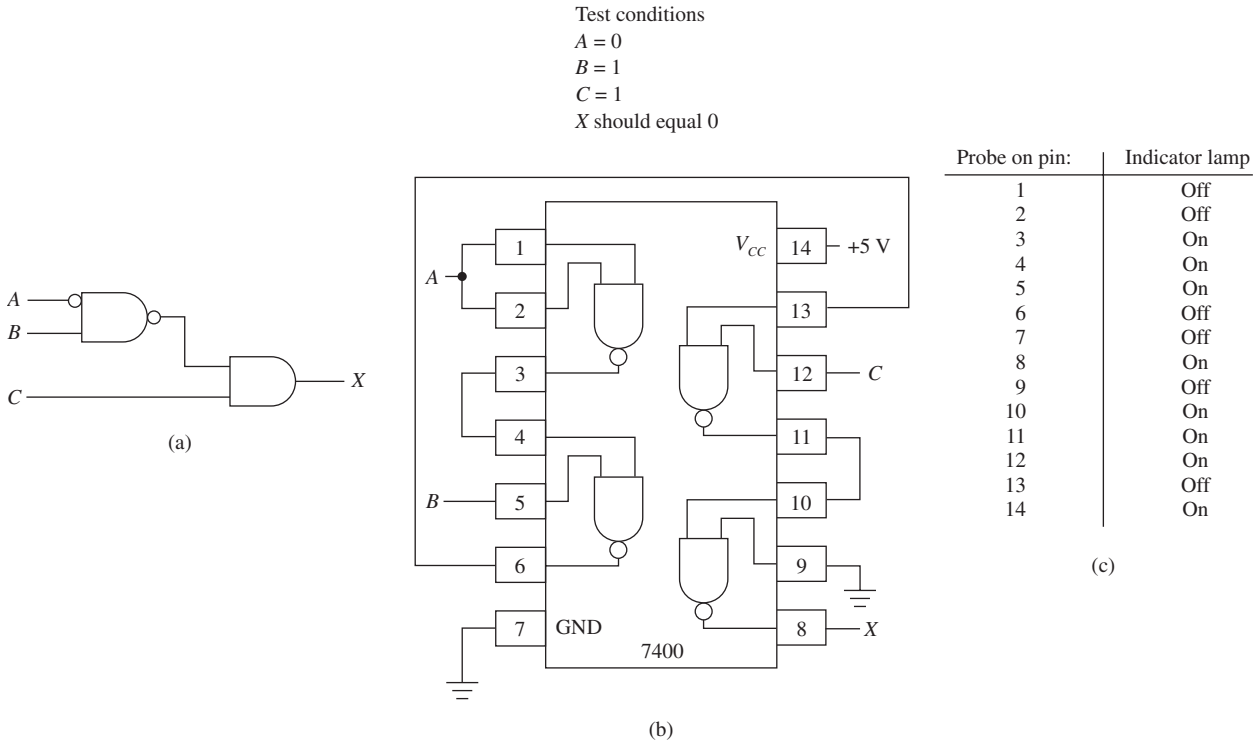
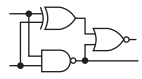



**Figure P5–43**

## Schematic Interpretation Problems



See Appendix G for the schematic diagrams.

**S** **5–44.** Find U8 in the HC11D0 schematic. Pins 11 and 12 are unused so they are connected to $V_{CC}$. What if they were connected to ground instead?

**S** **5–45.** Find U1:A in the Watchdog Timer schematic. This device is called a flip-flop and is explained in Chapter 10. It has two inputs, $D$ and CLK, and two outputs, $Q_A$ and $\overline{Q}_A$. Write the Boolean equation at the output (pin 3) of U2:A.

**S** **5–46.** Write the Boolean equation at the output (pin 3) of U12:A in the Watchdog Timer schematic. (*Hint:* Use the information given in Problem 5–45.)

**C** **S** **5–47.** Locate the U14 gates in the 4096/4196 schematic.

**(a)** Write the Boolean equation of the output at pin 6 of U14.

**(b)** What kind of gate does it turn into if you use the bubble-pushing technique?

**(c)** This is a 74HC08. What kind of logic gate is that?

**(d)** Complete the following sentence: Pin 3 of U14:A goes LOW if _____ OR if _____.

**C** **S** **5–48.** U10 of the 4096/4196 schematic is a RAM memory IC. Its operation is discussed in Chapter 16. To enable the chip to work, the Chip Enable input at pin 20 must be made LOW. Write a sentence describing the logic operation that makes that line go LOW. (*Hint:* Pin 20 of U10 goes LOW if _____.)