**NASSAU COMMUNITY COLLEGE**
Dean of Instruction Office

Revised Date: Fall 2015
Semester Offered: Fall/Spr/Sum

| | | | |
|---|---|---|---|
| ENS/PHY/TECH | September 2005 | | |
| Dept. (s) Offering Course | Effective Date | | |
| YES | | ELT113 | Course Offered On Campus **X** Off Campus |
| Degree Requirement | Prerequisite | Corequisite | |
| Digital I | ELT | | 214 . |
| Course Title | Dept. Prefix | Dual Listing | Course Number |

| | | | | |
|---|---|---|---|---|
| 3 | 0 | 3 | 3 | DIGITAL 1 |
| Lect.Hrs. | *Lab Hrs. | Contact | Credit | Course Title Abbreviation(10) |
| No | | No | | |
| Interdisciplinary | | Team Taught | | Brief Description of Special Procedure (Clarify also under Step 3 Potential Enroll) |

No .
Computer Usage ( If Yes, attach the computer utilization form)

Registrar (Certification of Code, Hours, Credits, Etc.)
*Lab hours may also refer to field work, clinical, studio or workshop hours.

What restrictions, if any, will limit eligibility for registering for the course? MAJORS ONLY

Textbook title, author, publisher, date: Digital Electronics a practical approach with VHDL
Current Ed. Kleitz, Pearson

Catalog Description: (include prerequisites and corequisites and special requirements that entail particular registration choice or extra expense for the student.) e.g. "lab fee applies"

**ELT 214: Digital I** 3 cr.
Corequisite: ELT 113
An introduction to Boolean algebra, Karnaugh minimization and the analysis/design of digital networks including arithmetic circuits, counters, registers and memories. In addition, basic hardware items such as multivibrators, Schmitt triggers and integrated circuits are analyzed.

Course Coordinator: Chris Atwood Dept. Chair: _____ Date: 1/13/16

**ELT 214 - COURSE OUTLINE**

OBJECTIVES

General

This course is designed to help begin the preparation of students in a technological career. ELT 214 is the first in a sequence of courses comprising the study of digital logic. The treatment of the subject material is presented in the language of Boolean mathematics. The student will learn the analysis, design and applications of digital logic circuits, including the basics of binary arithmetic and Boolean logic. The implementation of these mathematical functions using SSI and MSI integrated circuits will be explained including examples of actual commercially available circuits. These functions will then be combined to form more complex combinatorial and sequential logic.

Specific

***SEE ASSESSMENT MATRIX***

# ELT 214 - COURSE OUTLINE
# WEEKLY LECTURE TOPICS

| WEEK | DESCRIPTION |
|---|---|
| 1 | Introductory Digital Concepts; digital vs. analog: basic logic functions. |
| 1-3 | Number Systems & Codes<br>Number systems: decimal, binary, hex, octal; Conversion of bases: positional value, division, Binary & Hex Addition and 2's compliment; Subtraction, signed numbers(offset binary & 2's compliment signed binary notation); Numeric codes: BCD & Gray (lightly); Alphanumeric codes: ASCII, parity. |
| 3-4 | Basic Logic Gates<br>Inverter/, AND, OR, NAND, NOR; Truth tables, Boolean Symbols, Schematic Symbols, examples of interconnecting gates, exclusive OR & Exclusive NOR, programmable logic. |
| 5-7 | Logic Circuit Development; Boolean Operations; DeMorgan's Theorem; Standard Formats: SOP & POS; Karnaugh Map Simplification: SOP; Implementing Combinational Logic; Universal Property of NAND & NOR; Operation with pulse waveforms, programmable logic. |
| 8-9 | Functions of Combinational Logic<br>Arithmetic Circuits; Half & Full Adders; Parallel Binary Adders; Ripple carry vs. look-ahead; Comparators; Decoders & Encoders, & Code converters; Multiplexers;<br>Parity Generators/Checkers; Programmable logic (as an overview). |
| 10-11 | Sequential Logic: Flip-Flops<br>Latches and flip-flops, level and edge triggering; Master-Slave Operating Characteristics & Applications. |
| 12-13 | Sequential Logic: Counters<br>Asynchronous/Synchronous; Up/Down; Cascaded and applications. |
| 13-14 | Sequential Logic: Shift Registers<br>Serial In/Out - Parallel In/Out; Bi-directional; Applications & Counters |
| 15 | Memories<br>Basics; ROM - RAM – FLASH; Memory expansion.<br>Final Exam |

Note: Tests and/or quizzes are administered at regular intervals throughout the semester, the number of which is based upon the individual instructor's syllabus/course policy.